the ground via resistor **346** and switch **345**. Thus, the resistance value of resistor **346** controls the rate of discharge of capacitances **312** and **314**.

[0025] Still further, as shown in FIG. **3***a*, capacitor **334** is coupled to the gate of MOSFET **310** and helps to control the rate of discharge of capacitances **312** and **314**, because as shown in FIG. **3***a*, capacitor **334** is coupled to resistor **346** in parallel with parasitic capacitances **312** and **314**, and as such, when charged, provides a voltage potential that must flow through resistor **346** to ground, thereby affecting, for example, slowing, the rate of discharge of capacitances **312** and **314**.

[0026] Furthermore, switch **323** may be controlled by control circuitry to control the temporal application of voltage of voltage supply **322** to MOSFET **310**. For example, control circuitry may be configured to cause switch **323** to couple voltage supply **322** to MOSFET **310** earlier than otherwise to reduce the overall voltage stress on MOSFET **310** and reduce the relative resistance of resistor **311** (the drain-source resistance).

[0027] FIGS. **3***b*-**3***e* are equivalent circuit diagrams to system **300***a* of FIG. **3***a* at different temporal stages of operation of system **300***a*. Furthermore, FIG. **4** provides a graph **400** of the voltages across capacitances **312**, **314**, and **316** at different temporal stages of operation of system **300***a*, and will be discussed in conjunction with FIGS. **3***a*-**3***e*.

[0028] System **300***b* of FIG. **3***b* is the equivalent circuit to system **300***a* when voltage supply **322** is disconnected from system **300***a* by switch **323** (or the voltage regulator **105** is turned off via control circuitry **102** as shown in **200**), control voltage **342** is not shorted to ground by switch **345** and resistor **344**, and MOSFET **310** is going to off (due to the application of control voltage **342**). This state is illustrated in FIG. **4** from 10-20 milliseconds (mS). In this state, charge from control voltage **342** flows though resistances **344** and **346** to charge parasitic capacitances **312** and **314**, and a corresponding voltage is applied to parasitic capacitances **312** and **314** as illustrated by the rising voltages **313** and **315** of graph **400**. Control voltage **342** is disjoint with regard parasitic capacitance **316** and there is not voltage potential formed by control voltage **342** with regard to parasitic capacitance **316**, and therefore voltage **317** is zero, as illustrated from 10-20 milliseconds of graph **400**. The combination of resistors **344** and **346** slow the increase of voltage **313** (gate-source voltage), and pull down the voltage value of control voltage **342**, thereby helping to reduce voltage **313** over the illustrated 10-20 milliseconds of graph **400**.

[0029] System **300***c* of FIG. **3***c* is the equivalent circuit to system **300***a* when voltage supply **322** is connected to system **300***a* by switch **323** (more particularly, the source of MOSFET **310**) and control voltage **342** is not shorted to ground by switch **345** (and therefore control voltage **342** is applied to the gate of MOSFET **310**, ensuring that MOSFET **310** is off). This state is illustrated in FIG. **4** from 20-100 milliseconds (mS). With regard to voltage **313** (the gate source voltage of MOSFET **310**), after a transitory phase, in which voltage **313** drops with the addition of voltage supply **322** to a voltage value of the voltage value of voltage control **342** minus voltage supply **322** (voltage control **342**-voltage **322**), voltage **313** increases asymptotic to a voltage value as in graph **400**. In other words, the voltage applied to parasitic capacitance **312** drops to control voltage **342** minus voltage **322**, then rises asymptotic to a voltage.

[0030] Meanwhile, in system **300***c*, voltage **315** continues to increase asymptotic to the voltage value of voltage supply **322** such that parasitic capacitance **314** charges to the voltage value of voltage supply **322**. This is shown by the rising asymptotic voltage **315** of graph **400**. Simultaneously, voltage **317** drops to a negative value, as illustrated in graph **400**.

[0031] System **300***d* of FIG. **3***d* is the equivalent circuit to system **300***a* when voltage supply **322** is connected to system **300***a* by switch **323** (more particularly, the source of MOSFET **310**) and control voltage **342** is shorted to ground by switch **345**, thereby removing the voltage of control voltage **342** from the gate of MOSFET **310**. This state is illustrated in FIG. **4** from 100-160 milliseconds (mS). Since MOSFET **310** is an active control P-type FET, the control voltage is **342** is no longer applied to the gate of MOSFET **310**, but is shorted to ground, MOSFET **310** turns on and a channel resistance **311** is formed between drain and source. As can be seen from graph **400**, voltage **313** drops below zero and is asymptotic with a negative voltage value as the polarity of charge applied across parasitic capacitance **312** reverses as voltage supply **322** becomes the only voltage supply with the removal of control voltage **342** by shorting to ground.

[0032] Similarly, as can be seen from graph **400**, voltage **315** drops below zero and is asymptotic with the negative voltage value as the polarity of charge applied across parasitic capacitance **314** reverses as voltage supply **322** becomes the only voltage supply with the removal of control voltage **342** by shorting to ground. As would be understood by one of skill in the art, due to the shorting of control voltage **342** to ground, parasitic capacitances (the parasitic capacitances of the gate of MOSFET **310**) discharge with current flowing through resistor **346** to ground (resistor **344** being shorted to ground with control voltage **342**). Consequently, as discussed above, the resistance value of resistor **346** controls the discharge of parasitic capacitances **312** and **314**, and therefore helps control the voltage swings across the gate and source and the gate and drain of MOSFET **310**.

[0033] As can be further seen from graph **400**, voltage **317** rises from the negative voltage value to zero as MOSFET **310** turns on and the channel between the source and drain becomes active. The opening of the channel reduces parasitic capacitance **316** (between source and drain) to zero such that voltage **717** across parasitic capacitance **316** asymptotes to zero.

[0034] System **300***e* of FIG. **3***e* is the equivalent circuit to system **300***a* when voltage supply **322** is connected to system **300***a* by switch **323** (more particularly, the source of MOSFET **310**) and control voltage **342** is not shorted to ground by switch **345**, and therefore a voltage is applied to the gate of MOSFET **310**. This state is illustrated in FIG. **4** from 160 milliseconds (mS) forth. Since MOSFET **310** is an active control P-type FET, and since control voltage is **342** is applied to the gate of MOSFET **310**, and is no longer shorted to ground, MOSFET **310** is turning off and the channel between drain and source is fading. As can be seen from graph **400**, voltage **317** drops below zero as the channel between source and drain fades, and parasitic capacitance **316** (between source and drain) forms which is negatively charged by the combination of control voltage **342** and voltage supply **322**.

[0035] As can further be seen from graph **400**, voltages **313** and **315** rise from the negative voltage value to asymp-